AMENDMENTS TO SPECIFICATION

Please amend the following paragraph in the specification as indicated.

[0022] The first processing unit 102 is connected to the flash device(s) 106 and a communications port 104. While the description of the embodiments of the present invention makes reference to processors and processing units, it will be understood that the description pertains to processors, microprocessors, processing units and the like and the invention is not limited thereto. The first processing unit 102 is also connected to the local data bus 110, which is connected to the logic device 108 and the plurality of volatile memory devices 114, 124. The programmable logic device 108 is a programmable integrated circuit that allows the user of the circuit, using software control, to customize the logic functions the circuit will perform. In this case, the programmable logic device is controlled by the first processing unit 102 to provide output enable signals to the volatile memory devices and reset control lines to the processors 112 and 122. The programmable logic device also receives volatile/non-volatile output enable control signals 120 from each second processing unit 112, 122. The programmable logic device 108 can be a complex programmable logic device (CPLD), a field programmable gate array (FPGA), or the like. Each second processing unit 112, 122 is connected to its associated volatile memory device 114, 124 by the data busses 116 and 126, respectively. The volatile memory devices can be static random access memory devices, dual port random access memory devices, or the like. A pulldown network 119, 129 is connected between each data bus 116, 126 and ground. This resistor network insures that the data bus is at a zero state when the bus is in tristate mode. Thus, when the second processor reads the data bus at a zero state, it is a no-op command to the processor. This method is needed for synchronous volatile memory since the processor during power-up does not supply the clock 113, 123 for about 10 execution cycles that is needed to read data from synchronous memory. The no-op command is a `filler` for this interval until the processor produces the clock 113, 123.